

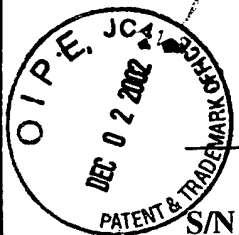
2818

First Named Inventor	S. Derner	<b>TRANSMITTAL</b> UNDER §1.8  (LARGE ENTITY)
Serial No.	10/017,658	
Filing Date	December 12, 2001	
Group Art Unit	2818	
Examiner Name	Tan Nguyen	
Attorney Docket No.	400.105US01	
Title: HALF DENSITY ROM EMBEDDED DRAM		

Commissioner for Patents  
BOX NON-FEE AMENDMENT  
Washington, DC 20231

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<b>Enclosures</b>					
<b>The following documents are enclosed:</b>					
X An Amendment and Response to Office Action (6 pgs., including Marked Version);					
X A return postcard.					
Please charge any additional fees or credit any overpayments to Deposit Account No. 501373.					
<b>CUSTOMER NO. 27073</b>					
<b>Submitted By</b>					
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Signature				Date	11/26/02
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<b>Certificate of Mailing</b>					
I certify that this correspondence, and the documents identified above, are being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, Washington, D.C. 20231 on <u>November 26, 2002</u> .					
Name	Susan W. Donovan	Signature			



S/N 10/017,658

PATENT

*W. A. Sosa*  
12/31/02

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

First Named

Inventor: Scott Derner

Examiner: Tan Nguyen

Serial No.: 10/017,658

Group Art Unit: 2818

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Title: HALF DENSITY ROM EMBEDDED DRAM

**AMENDMENT AND RESPONSE**

Commissioner for Patents  
Washington, D.C. 20231

In response to the Office Action dated September 13, 2002, please amend the above-identified patent application as follows:

**IN THE SPECIFICATION**

In the specification, please amend paragraph 0024 to read as follows:

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a1  
[0024] Numerous methods are available to program the ROM cells. For example, U.S. Patent No. 6,134,137 issued October 17, 2000 entitled "ROM-EMBEDDED-DRAM" describes ROM cells that are fabricated to short the memory cell to either its wordline or an adjacent wordline. Shorting the memory cell to its wordline results in reading a logic one (Vcc). Shorting the memory cell to an adjacent wordline results in reading a logic zero (Vss). Shorting a cell to its own wordline, however, may result in a digit line to wordline short during fabrication. As such, hard programming logic zeros may only be possible for some fabrication layouts. The hard programming technique of U.S. Patent No. 6,134,137 is an example of a technique for programming ROM cells using a DRAM fabrication. Other techniques for programming a ROM cell using a DRAM fabrication can be used without departing from the present invention. For example, ROM cells can be hard programmed by eliminating cell dielectric so that the cell plates are shorted to a program voltage, an electrical plug can be fabricated between the cell plates and shorted to a program voltage, the ROM cell can be